Applicant	Bogdan M. Duduman	**AMENDMENT UNDER 37 C.F.R. §1.312**
Serial No.	09/552,117	
Filing Date	April 19, 2000	
Group Art Unit	2857	
Examiner Name	Elias Desta	
Confirmation No.	3110	
Attorney Docket No.	125.037US01	
Title: ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS		

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Please amend the above-identified application as follows:

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 9 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of claims:

1. (Previously presented) An integrated circuit for monitoring and controlling multiple power outputs from a power supply that generates a first primary power voltage and one of more secondary primary power voltages, comprising:

an input means for receiving the first primary and secondary primary power voltages to generate controlled voltage power outputs;

means for comparing a signal representative of the first primary power voltage to a reference signal;

means for sensing when the first primary power voltage reaches or exceeds a threshold reference level;

means for delaying connection of the first primary and secondary primary power voltages to the controlled voltage power outputs for a selected delay time after the first primary power voltage reaches the reference threshold level.; and

means for initiating a soft start after the selected delay time has expired.

2. (Original) The integrated circuit of claim 1 further comprising means for generating a power up signal for indicating that all the monitored output voltages of the monitored power supply are at or above a useable and effective voltage level.

3. (Previously presented) The integrated circuit of claim 1 wherein the means for comparing comprises a voltage divider and a comparator, wherein the comparator is coupled to a threshold reference voltage and the voltage divider is coupled to the first primary power voltage and to the comparator.

4. (Original) The integrated circuit of claim 3 wherein the delaying means comprises a timing circuit and the output of the comparator is coupled to the timing circuit for delaying connection of the input power supply voltages to the controlled outputs for the selected delay time.

5. (Original) The integrated circuit of claim 1 further comprising a linear controller for controlling the output voltage of each of the power output voltages of the power monitor circuit.

6. (Previously presented) A computer system with monitored power comprising in combination:

a power supply for generating a first primary dc power voltage and one or more secondary primary dc power voltages, a motherboard comprising multiple units including a memory unit and a central processing unit, wherein said units may require different operating voltages; and a power monitoring integrated circuit disposed between the power supply and the motherboard for controlling supply power from the power supply to the mother board, said power monitoring circuit comprising,

input means for receiving the first primary and secondary primary power voltages from the power supply;

means for controlling the received power voltages to generate controlled voltage power outputs;

means for comparing a signal representative of the first primary power voltage to a reference signal;

means for sensing when the first primary power voltage reaches or exceeds a threshold reference level; and

means for delaying connection of the controlled power output voltages to the computer for a selected delay time after the first primary power voltage reaches the reference threshold level, wherein the selected time delay insures the power output voltages are stabilized.

7. (Previously presented) The computer system of claim 6 further comprising means for generating a power up signal for indicating that all the monitored output voltages of the monitored power supply are at or above a usable and effective voltage level.

8. (Previously presented) The computer system of claim 6 wherein the means for comparing comprises a voltage divider and a comparator, wherein the comparator is coupled to a threshold reference voltage and the voltage divider is coupled to the first primary power voltage and to the comparator.

9. (Original) The computer system of claim 8 wherein the delaying means comprised a timing circuit and the output of the comparator is coupled to the timing circuit for delaying connection of the controlled power output voltages to the computer for the selected delay time.

10. (Original) The computer system of claim 6 wherein the means for controlling the output voltages comprises a plurality of linear controllers with each linear controller controlling the output voltage of one of the power output voltages of the power monitor circuit.

11. (Previously presented) A method for monitoring and controlling power from a power supply that generates a first primary power voltage and one or more secondary primary power voltages related to the first primary power voltage, comprising:

receiving the first and secondary primary power voltages from the power supply;

controlling the received power voltages to generate controlled voltage power outputs;

comparing a signal representative of the first primary power voltage to a reference signal;

sensing when the first primary power output voltage reaches or exceeds a threshold reference level; and

delaying connection of the power supply controlled voltage power outputs for a selected delay time after the first primary power output voltage reaches the reference threshold level.

12. (Previously presented) The method of claim 11 further comprising, generating an output signal indicating that the first primary power voltage has reached at least 90% of its target value.

13. (Previously presented) The method of claims 11, wherein the step of comparing a signal representative of the first primary power voltage to a reference voltage further comprises:

dividing a signal representative of the first primary power voltage and comparing the voltage divided signal to a threshold reference voltage.

14. (Previously presented) The method of claim 13 wherein the delaying step comprises timing an interval starting when the voltage divided signal exceeds the threshold reference signal and delaying connection of the controlled voltage power outputs to the computer for a selected delay time.

15. (Original) The method of claims 11 further comprising ~~linerally~~ linearly controlling each of the power output voltages of the power monitor circuit.

16. (Previously presented) A power monitor circuit comprising:

a first input adapted to receive a first primary voltage from a power supply;

one or more secondary inputs to receive one or more secondary primary voltages from the power supply, wherein the one or more secondary primary voltages are related to the first primary voltage;

a comparator circuit adapted to compare the first primary voltage with a reference voltage; and

a time delay circuit adapted to delay an output of the one or more secondary primary voltages by a select period of time once the first primary voltage equals or exceeds the reference voltage.

17. (Currently amended) The power monitor circuit of claim 16, wherein the comparator circuit further comprises:

a resistor divider network adapted to divide the first primary voltage, the resistor divider network comprising:

a first resistor of a first select value, and

a second resistor of a second select value, the first and second resistor being adapted to divide the first primary voltage into a select first divided primary voltage; and

a comparator having a first input coupled to the ~~resister~~ resistor divider network to receive the select divided first primary voltage, the comparator having a second input coupled to receive the reference voltage, the comparator further having an output coupled to the time delay circuit.

18. (Previously presented) The power monitor circuit of claim16, wherein the reference voltage is approximately equal to 90% of the first primary voltage.

19. (Previously presented) The power monitor circuit of claim 16, wherein the time delay circuit outputs the first primary and one or more secondary primary voltages approximately 40ms after the primary voltage equals or exceeds the reference voltage.

20. (Previously presented) The power monitor circuit of claim 16, wherein the first primary voltage is approximately equal to 12 volts, one of the secondary primary voltages

is approximately equal to 3.3 volts and another of the secondary primary voltages is approximately equal to 5 volts.

21. (Previously presented) A power monitor circuit for monitoring a voltage from a power supply wherein the power supply derives two or more associated voltages, the power monitor circuit comprising:

a first input adapted to receive one voltage of the two or more voltages from the power supply;

a secondary input for each of the remaining two or more voltages, each secondary input adapted to receive an associated one of the remaining two or more voltages;

an output for each of the two or more voltages;

a comparator circuit adapted to compare the one voltage received at the first input with a reference voltage; and

a time delay circuit adapted to delay the coupling of the two or more voltages to the outputs for a select period of time after the comparator has sensed the one voltage received on the first input equals or exceeds the reference voltage.

22. (Previously presented) The power monitor circuit of claim 21, wherein the one voltage received on the first input is a first primary voltage and the remaining two or more voltages are secondary primary voltages.

23. (Previously presented) The power monitor circuit of claim 21, wherein the reference voltage is in relation to 90% of the nominal setting of the one voltage received at the first input.

24. (Previously presented) The power monitor circuit of claim 21, wherein the select period of time is approximately 40ms.

25. (Previously presented) The power monitor circuit of claim 21, further comprising:

a voltage divider adapted to divide the one voltage received on the first input, wherein the divided one voltage received on the first input is compared to the reference voltage.

REMARKS

The amendments to claim numbers 15 and 17 are made to correct typos. If the Examiner has any questions or concerns regarding this application, please contact Scott V. Lundberg at 612-455-1690.

Respectfully submitted,

Date: 9-20-04

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Receipt of the below-listed documents is here . acknowledged in the U.S. Patent and Trademark Office:

Applicant: Bogdan M. Duduman
Serial No.: 09/552,117
Filing date: April 19, 2000
Title: ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS

Allowed: April 22, 2004
Confirmation No.: 3110

Enclosed: Issue Fee Transmittal in duplicate; Credit Card Payment Form (1 pg.) for Issue Fee; Amendment Under 37 C.F.R. 1.312 (9 pgs.); and Transmittal document.

Receipt of the below-listed documents is hereby acknowledged in the U.S. Patent and Trademark Office:

Applicant: Bogdan M. Duduman
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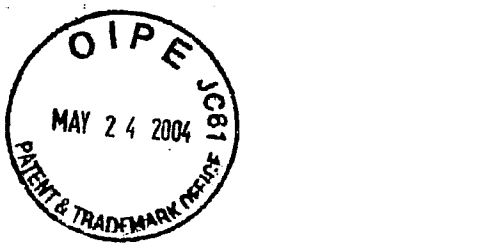
Enclosed: Issue Fee Transmittal in duplicate; Credit Card Payment Form (1 pg.) for Issue Fee; Amendment Under 37 C.F.R. 1.312 (9 pgs.); and Transmittal document.

Mailed via First Class Mail: May 20, 2004
Attorney Docket No.: 125.037US01
SVL:eab



During sleep to active state transitions from conditions where the outputs are initially 0V (such as S4/S5 to S0 transition with EN3VDL=1 and EN5VDL=0, or simple power-up sequence directly into active state), the 3V DUAL and 5V DUAL outputs go through a quasi soft-start by being pulled high through the body diodes of the N-channel MOSFETs connected between these outputs and the 3.3V and 5V ATX outputs, respectively, FIG. **5** shows this start-up scenario.

5V SB is already present when the main ATX outputs are turned on at a time T0. Similarly, the soft-start capacitor has already been charged up to 1.25V and the clamp is active, awaiting for the 12V power-on reset (POR) timer to expire. As a result of 3.3V IN and 5V IN ramping up, the 3.3V DUAL and 5V DUAL output capacitors C1, C3 charge up through the body diodes of Q3 and Q5, respectively (see FIG. **3**). At time T1, the 12V ATX output exceeds the 12V undervoltage threshold of circuit **22**, and the internal 50ms (typical) timer **25** (FIG. **2**) is initiated. At T2 the time-out initiates a soft-start, and the memory output is ramped-up, reaching regulation limits at time T3. Simultaneous with the memory voltage ramp-up, the DLA output **321** is pulled high (to 12V), turning on Q3 and Q5, and bringing the 3.3V DUAL and 5V DUAL outputs in regulation at time T2. At time T4, when the soft-start voltage reaches approximately 2.8V, the undervoltage monitoring circuits are enabled and the soft-start capacitor is quickly discharged to approximately 2.45V.

Requests to go into a sleep state during an active state soft-start ramp-up result in a chip reset, followed by a new soft-start sequence into the desired state.

Having thus disclosed the preferred embodiment of the invention, those skilled in the art will appreciate that further modifications, changes and omissions of one or more elements to the preferred embodiment may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. An integrated circuit for monitoring and controlling multiple power outputs from a power supply that generates a first primary power voltage and one of more secondary primary power voltages, comprising:

an input means for receiving the fist primary and secondary primary power voltages to generate controlled voltage power outputs;

means for comparing a signal representative of the first primary power voltage to a reference signal;

means for sensing when the first primary power voltage reaches or exceeds a threshold reference level;

means for delaying connection of the first primary and secondary primary power voltages to the controlled voltage power outputs for a selected delay time after the first primary power voltage reaches the reference threshold levels; and

means for initiating a soft start after the selected delay time has expired.

2. The integrated circuit of claim **1** further comprising means for generating a power up signal for indicating that all the monitored output voltages of the monitored power supply are at or above a useable and effective voltage level.

3. The integrated circuit of claim **1** wherein the means for comparing comprises a voltage divider and a comparator, wherein the comparator is coupled to a threshold reference voltage and the voltage divider is coupled to the first primary power voltage and to the comparator.

4. The integrated circuit of claim **3** wherein the delaying means comprises a timing circuit and the output of the comparator is coupled to the timing circuit for delaying connection of the input power supply voltages to the controlled outputs for the selected delay time.

5. The integrated circuit of claim **1** further comprising a linear controller for controlling the output voltage of each of the power output voltages of the power monitor circuit.

6. A computer system with monitored power comprising in combination:

a power supply for generating a first primary do power voltage and one or more secondary primary dc power voltages, a motherboard comprising multiple units including a memory unit and a central processing unit, wherein said units may require different operating voltages; and a power monitoring integrated circuit disposed between the power supply and the motherboard for controlling supply power from the power supply to the mother board, said power monitoring circuit comprising,

input means for receiving the first primary and secondary primary power voltages from the power supply;

means for controlling the received power voltages to generate controlled voltage power outputs;

means for comparing a signal representative of the first primary power voltage to a reference signal;

means for sensing when the first primary power voltage reaches or exceeds a threshold reference level; and

means for delaying connection of the controlled power output voltages to the computer for a selected delay time after the first primary power voltage reaches the reference threshold level, wherein the selected time delay insures the power output voltages are stabilized.

7. The computer system of claim **6** further comprising means for generating a power up signal for indicating that all the monitored output voltages of the monitored power supply are at or above a usable and effective voltage level.

8. The computer system of claim **6** wherein the means for comparing comprises a voltage divider and a comparator, wherein the comparator is coupled to a threshold reference voltage and the voltage divider is coupled to the first primary power voltage and to the comparator.

9. The computer system of claim **8** wherein the delaying means comprised a timing circuit and the output of the comparator is coupled to the timing circuit for delaying connection of the controlled power output voltages to the computer for the selected delay time.

10. The computer system of claim **6** wherein the means for controlling the output voltages comprises a plurality of linear controllers with each linear controller controlling the output voltage of one of the power output voltages of the power monitor circuit.

11. A method for monitoring and controlling power from a power supply that generates a first primary power voltage and one or more secondary primary power voltages related to the first primary power voltage comprising:

receiving the first and secondary primary power voltages from the power supply;

controlling the received power voltages to generate controlled voltage power outputs;

comparing a signal representative of the first primary power voltage to a reference signal;

sensing when the first primary power output voltage reaches or exceeds a threshold reference level; and

delaying connection of the power supply controlled voltage power outputs for a selected delay time after the first primary power output voltage reaches the reference threshold level.

12. The method of claim 11 further comprising, generating an output signal indicating that the first primary power voltage has reached at least 90% of its target value.

13. The method of claims 11, wherein the step of comparing a signal representative of the first primary power voltage to a reference voltage her comprises:

dividing a signal representative of the first primary power voltage and comparing the voltage divided signal to a threshold reference voltage.

14. The method of claim 13 wherein the delaying step comprises timing an interval starting when the voltage divided signal exceeds the threshold reference signal and delaying connection of the controlled voltage power outputs to the computer for a selected delay time.

15. The method of claims 11 further comprising linearly controlling each of the power output voltages of the power monitor circuit.

16. A power monitor circuit comprising:

a first input adapted to receive a first primary voltage from a power supply;

one or more secondary inputs to receive one or more secondary primary voltages from the power supply, wherein the one or more secondary primary voltages are related to the first primary voltage;

a comparator circuit adapted to compare the first primary voltage with a reference voltage; and

a time delay circuit adapted to delay an output of the one or more secondary primary voltages by a select period of time once the first primary voltage equals or exceeds the reference voltage.

17. The power monitor circuit of claim 16, wherein the comparator circuit further comprises:

a resistor divider network adapted to divide the first primary voltage the resistor divider network comprising:

a first resistor of a first select value, and

a second resistor of a second select value, the first and second resistor being adapted to divide the first primary voltage into a select first divided primary voltage; and

a comparator having a first input coupled to the resistor divider network to receive the select divided fir;m primary voltage, the compressor having a second input coupled to receive the reference voltage, the comparator fiber having an output coupled to the time delay circuit.

18. The power monitor circuit of claim 16, wherein the reference voltage is approximately equal to 90% of the first primary voltage.

19. The power monitor circuit of claim 16, wherein the time delay circuit outputs the first primary and one or more secondary primary voltages approximately 40 ms after the primary voltage equals or exceeds the reference voltage.

20. The power monitor circuit of claim 16, wherein the first primary voltage is approximately equal to 12 volts, one of the secondary primary voltages is approximately equal to 3.3 volts and another of the secondary primary voltages is approximately equal to 5 volts.

21. A power monitor circuit for monitoring a voltages from a power supply wherein the power supply derives two or more associated voltages, the power monitor circuit comprising:

a first input adapted to receive one voltage of the two or more voltages from the power supply;

a secondary input for each of the remaining two or more voltages; each secondary input adapted to receive an associated one of the remaining two or more voltages;

an output or each of the two or more voltages;

a comparator circuit adapted to the one voltage received at the first input with a reference voltage; and

a time delay circuit adapted to delay the coupling of the two or more voltages to the outputs for a select period of time after the comparator has sensed the one voltage received on the first input equals or exceeds the reference voltage.

22. The power monitor circuit of claim 21, wherein the one voltage received on the first input is a first primary voltage and the remaining two or more voltages are secondary primary voltages.

23. The power monitor circuit of claim 21, wherein the reference voltage is in reaction to 90% of the nominal setting of the one voltage received at the first input.

24. The power monitor circuit of claim 21, wherein the select period of time is approximately 40 ms.

25. The power monitor circuit of claim 21, further comprising:

a voltage divider adapted to divide the one voltage received on the first input, wherein the divided one voltage received on the first input is compared to the reference voltage.

* * * * *

PTO/SB/44 (06-07)
Approved for use through 06/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,882,942
APPLICATION NO. : 09/552,117
ISSUE DATE : 4/19/2005
INVENTOR(S) : Duduman

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At Claim 1, Column 5, Line 43, please replace “fist” with “first”

At Claim 1, Column 5, Line 54, please replace “levels” with “level”

At Claim 6, Column 6, Line 9, please replace “do” with “dc”

At Claim 11, Column 6, Line 54, please add a “,” after “voltage”

At Claim 13, Column 7, Line 6, please replace “her” with “further”

At Claim 17, Column 7, Line 35, please add a “,” after “voltage”

At Claim 17, Column 7, Line 43, please replace “fir;m” with “first”

At Claim 17, Column 7, Line 44, please replace ”compressor” with “comparator”

MAILING ADDRESS OF SENDER(Please do not use customer number below):

Fogg & Powers LLC
10 South Fifth Street, Suite 1000
Minneapolis, MN 55402

PTO/SB/44 (06-07)
Approved for use through 06/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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APPLICATION NO. : 09/552,117
ISSUE DATE : 4/19/2005
INVENTOR(S) : Duduman

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At Claim 17, Column 7, Line 46, please replace “fiber” with “further”

At Claim 21, Column 8, Line 23, please replace “or” with “for”

At Claim 21, Column 8, Line 24, please add “compare” after “to”

At Claim 23, Column 8, Line 36, please replace “reaction” with “relation”

MAILING ADDRESS OF SENDER(Please do not use customer number below):

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10 South Fifth Street, Suite 1000
Minneapolis, MN 55402

Applicant	Duduman	**COMMUNICATION REGARDING CERTIFICATE OF CORRECTION**
Patent No.	6,882,942	
Issue Date	4/19/2005	
Serial No.	09/552,117	
Attorney Docket No.	125.037US01	
Title: ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS		

ATTN: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant hereby requests issuance of a Certificate of Correction in U.S. Letters Patent No. 6,882,942 as specified on the attached Certificate (Form PTO/SB/44). Please find enclosed documentation supporting errors identified in the above noted patent, referred to herein as Exhibits A and B.

With respect to the errors identified in the claims of the issued patent, Exhibit A is a copy of the claims of the issued patent, and Exhibit B comprises a listing of the claims filed in an amendment under 37 CFR § 1.312 and a corresponding postcard receipt indicating receipt of said amendment at the U.S. Patent & Trademark Office on May 24, 2004. The identified errors constitute typographical errors, and, as such, do not introduce new matter.

Applicant believes these corrections as specified are due to an Office error and therefore does not believe that any fee is due for issuance of a Certificate of Correction. However, if deemed necessary, the Office is authorized to charge any additional fees found due to Deposit Account No. 502432. Please contact the undersigned if there are any further questions.

Respectfully submitted,

Date: August 29, 2007

/David D. Freitag/

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